Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application. All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claims is indicated in parenthetical expression following the claim number.

Claims 1-8 remain.

Claim 2 has been allowed.

Claims 1, 4, and 7-8 are being amended.

Claim 3 is being cancelled.

WHAT IS CLAIMED IS:

1. (Currently Amended) An integrated circuit comprising:

a. an analog to digital converter;

b. a finite impulse response (FIR) filter; and

c. an output mechanism selectively providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data, the output mechanism comprising one or more bits of a register of the integrated circuit which a user can set to control the selection of the fully settled data from the FIR filter or all of the data from the FIR filter, including the unsettled data.

2. (Previously Presented) An integrated circuit comprising:

a. an analog to digital converter;

b. a finite impulse response (FIR) filter; and

c. an output mechanism selectively providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data in which the output mechanism comprises an external pin on the integrated circuit to which a user can apply a control signal to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

3. (Cancelled)

4. (Currently Amended) The integrated circuit of claim 1 [[3]] in which said one or more bits of [[on]] a register of the integrated circuit are set over a serial port interface.

5. (Original) The integrated circuit of claim 1 in which the analog to digital converter is a delta sigma modulator.

6. (Original) The integrated circuit of claim 1 in which the FIR filter is a decimation filter.

7. (Currently Amended) A method of designing an integrated circuit having a finite impulse response (FIR) filter, comprising the step of providing a[[n]] mechanism including an external pin on the integrated circuit to which a user can apply a control signal to permit the [[a]] user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

8. (Currently Amended) A method of fabricating an integrated circuit having a finite impulse response (FIR) filter, comprising the step of providing a[[n]] mechanism including one or more bits of a register of the integrated circuit to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.